INTEGRATED DEVICE IN EMITTER-SWITCHING CONFIGURATION AND RELATED MANUFACTURING PROCESS

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention refers to an integrated device in emitter-switching configuration and related manufacturing process.

Description of the Related Art

Among the different integrated devices in emitter-switching configuration there is a particular type that is constituted by a high voltage power bipolar transistor and by a low voltage signal transistor where the emitter terminal of the power transistor is connected with the charge collection terminal (drain or collector) of the low voltage transistor. Generally the power transistor has a Breakdown voltage that can exceed 1kV and it must be able to commutate at high frequencies (at about 200khz). The low voltage transistor has a Breakdown voltage lower than 60V and it has fast commutation features that assure the use of the emitter switching device at high frequencies.

An example of a device in emitter-switching configuration is shown in Figure 1. Such a device comprises a high voltage bipolar transistor Th and a MOS or bipolar low voltage device, indicated schematically by a block 1. The emitter terminal of the transistor Th is connected with the charge collection terminal (drain or collector) of the low voltage transistor 1. The base terminal Bh and the terminal C (base terminal or gate terminal of the transistor 1) constitute the control terminals of the device, which allow the connection between two circuit parts connected with the terminal Ch (collector terminal of the transistor Th) and Ee (emitter or source terminal of the transistor 1) which can be opened and closed alternately. Generally the terminal Ee is connected with ground, the terminal Ch is connected with a first terminal of a load L the second terminal of which is connected with a supply voltage Vcc. The device comprises a quenching element B

constituted, for example, by a Zener diode or by a series of diodes which is connected between the terminals Bh and Ee.

During the turning on of the device, the quenching time of the transistor Th is greater than the quenching time of the transistor 1 because of the large accumulation of charges in the base of the transistor Th. After the transistor 1 is quenched, bringing the emitter current of the transistor Th to zero, a current flows from the collector of the transistor Th through its base and this current is discharged to ground through the quenching element B. Once all the charge residuals in the base of the transistor Th have been eliminated, its collector current, and hence the current in the load L, is brought to zero.

In known devices in emitter-switching configuration, the quenching element is formed, for example, by discrete components suitably connected with the two transistors; this solution increases the production cost and the size of the device.

In the case wherein both the high voltage transistor and the low voltage transistor are integrated in the same semiconductor chip, the quenching element is normally formed within an insulated well of the region wherein the control circuits are allocated.

A different solution is disclosed in US 6127723 where an integrated device in emitter-switching configuration is disclosed comprising a high voltage bipolar transistor and a low voltage transistor and wherein the quenching element, a Zener diode, is formed in the base region or in the emitter region of the high voltage bipolar transistor. In this way the integrated device occupies a limited space in the semiconductor chip and a low resistance in series with the quenching element is assured so that the power dissipation at the quenching stage is reduced.

However this solution presents the disadvantage of reducing the whole area of the high voltage bipolar transistor and of the low voltage transistor in order to form the quenching element. In the case wherein the Zener diode is formed in the emitter region of the high voltage transistor, besides the reduction of the whole area of the low voltage transistor a reduction of the efficiency of the high voltage transistor in the zone underlying the Zener diode is achieved.

BRIEF SUMMARY OF THE INVENTION

The present invention provides an integrated device in emitter-switching configuration which shows a novel quenching element.

According to an embodiment of the present invention, an integrated device in emitter switching configuration is provided, said device being integrated in a chip of semiconductor material of a first conductivity type, said chip having a first surface and a second surface opposite to each other, said device comprising a first transistor having a base region, an emitter region and a collector region, a second transistor having a not drivable terminal for collecting charges which is connected with the emitter terminal of the first transistor, a quenching element of the first transistor which discharges current therefrom when said second transistor is turned off, said quenching element being coupled with the base terminal of the first transistor and with the other not drivable terminal of the second transistor, said quenching element comprising at least one Zener diode made in polysilicon, said at least one polysilicon Zener diode being formed on the second surface of said chip and comprising a polysilicon layer having at least one zone of the first conductivity type and at least one zone of a second conductivity type in order to form at least one P-N junction.

According to another embodiment of the present invention a process for manufacturing an integrated device in emitter-switching configuration is provided.

Thanks to the present invention it is possible to provide an integrated device in emitter-switching configuration which occupies a smaller space than the known devices and is particularly usable in the case wherein the collector terminal of the high voltage transistor assumes negative voltage values.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S)

The features and the advantages of the present invention will be made evident by the following detailed description of its particular embodiments, illustrated as not limiting examples in the annexed drawings, wherein:

Figure 1 is a circuit scheme of a device in emitter switching configuration according to prior art;

Figure 2 is a schematic cross-section of an integrated device in emitter-switching configuration according to a first embodiment of the invention;

Figure 3 is a circuit scheme of the device in Figure 2;

Figure 4 is a schematic cross-section of an integrated device in emitter-switching configuration according to a second embodiment of the invention;

Figure 5 is a circuit scheme of the device in Figure 4;

Figures 6A-6D show different quenching structures that can be used in the formation of the devices in Figures 2 and 4;

Figure 7 is a schematic cross-section of an integrated device in emitter-switching configuration according to a third embodiment of the invention;

Figure 8 is a circuit scheme of the device in Figure 7;

Figure 9 is a schematic cross-section of an integrated device in emitter-switching configuration according to a fourth embodiment of the invention;

Figure 10 is a circuit scheme of the device in Figure 9;

Figures 11A and 11B show circuit schemes of an integrated device in emitter-switching configuration according to a fifth embodiment of the invention;

Figure 12 is a diagram of the output features of the device in Figure 5 by imposing a voltage Vgs=10V.

DETAILED DESCRIPTION OF THE INVENTION

With reference to Figure 2 an integrated device in emitter-switching configuration is shown which is formed in a semiconductor substrate 2 having N-type dopant of a high concentration according to a first embodiment of the invention. The integrated device is formed, for example, by means of the VIPower process (VIPower is a trademark of the SGS-THOMSON MICROELECTRONICS S.r.l.) described in the US patent application 4,965,215 in the name of SGS-THOMSON MICROELECTRONICS S.r.l., and incorporated herein by reference, wherein the high voltage transistors have a

totally vertical conduction structure, wherein the different P-N junctions are buried and the collector electrode is formed on the bottom surface of the chip.

The semiconductor material chip wherein the integrated device is formed comprises on the substrate 2 a first epitaxial layer 3 with N-type dopant of a low concentration, which is formed on the substrate by means of an epitaxial growth. A P-type silicon region 4 is formed on the top surface of the epitaxial layer 3 by means of an ionic implant and successive diffusion; a region 5 with N-type dopant of a high concentration is formed on the P-type region 4. A second epitaxial layer 6 that has a dopant concentration higher than the first epitaxial layer is formed on the first layer by epitaxial growth. The high temperature of this process step allows the diffusion of the P and N type impurities inside the epitaxial layers 3 and 6.

P-type contact regions 7 extending through the whole epitaxial layer 6 and which are connected with the region 4, are then formed in the layer 6 by means of known technologies of masking, implant and diffusion so as to define a portion 8 of the epitaxial layer 6. N-type contact regions 9 with high dopant concentration which are connected with the region 5 are formed by similar technologies. At least one P-type region 10 is formed by means of similar implant and diffusion technologies (or alternatively by means of a deposition process) inside a portion 100 of the layer 6 which is delimited by the regions 9. An N-type region 11 is then implanted and diffused in the region 10.

In such way the transistors Th and Te have been formed which are present in the circuit configuration in Figure 3: in fact the regions 5, 4, 3 represent respectively the emitter, base and collector regions of the bipolar transistor Th and the regions 11, 10 and 100 represent respectively the emitter, base and collector regions of the bipolar transistor Te.

On the top surface 400 of the chip an insulated layer 12, typically silicon oxide, is deposited by using an appropriate masking. Successively, by means an appropriate masking, a polysilicon layer 14 on a silicon oxide region 13 placed over the region 9 and an adjacent portion of the layer 6 which is allocated between said region 9 and the region 7 on the left part of the chip as showing Figure 2.

Always using appropriate masking a doping of the whole polysilicon layer 14 with a P-type dopant (for example boron) and a successive doping with a N-type dopant (for example phosphorus) above some parts of the layers 14 in order to form one or more P-N junctions occurs. Alternatively the whole polysilicon layer 14 can be doped with an N type dopant (for example phosphorus) and successively with a P-type dopant only above some parts of the layer 14 in order to form one or more P-N junctions. Successively, by using an appropriate masking, a deposition of oxide 15 over the polysilicon layer 14 and an attack of the oxide layers 12 and 15 for forming the zones wherein the contacts of the transistors Th and Te and of the P-N junctions by means of a successive deposition of a metal layer 16 are formed occur. The one or more P-N junctions represent the quenching element B of the circuit scheme of Figure 3. If, for example, a single P-N junction has been formed as shown in Figure 2 and in Figure 6a, that is a single Zener diode, one of the two terminals Bh which are present in Figure 2 contacts both the region 7 and the N part of the P-N junction while the P part is contacted by the terminal Ee that contacts even the region 11. The terminal Be contacts the region 10. A collector electrode Ch is formed by a metal layer 200 on the below surface 300 of the substrate 2.

Instead of a single P-N and therefore of a single Zener diode Dz1 it is possible to form on the polysilicon layer 14 two P-N junctions in order to form two Zener diodes Dz1 and Dz2 in back to back connection, that is with anodes and cathodes which are united together as shown respectively in Figures 6b and 6c, or different P-N junctions in order to form different couples of Zener diodes Dz1...Dzn in back to back connection, as shown in Figure 6d.

In the top view the transistor Th presents typically a geometric shape called "interdigitated" wherein the emitter region extends as a comb having elongated portions (fingers) inside the base region. The structures of the polysilicon diodes which have been described are fit to be distributed along all the perimeter of the fingers of the transistor Th in order to obtain an optimal junction perimeter, even occupying the same space of an emitter-switching device without an integrated quenching element.

In Figure 4 a device in emitter switching configuration which is formed in the semiconductor substrate 2 with high N-type dopant concentration according to a second embodiment of the invention is shown. The integrated device of such second embodiment of the invention differs from the device of the first embodiment because of the presence of a MOS transistor as low voltage transistor. After the formation of the epitaxial layer 3 on the substrate 2 and the successive formation of the region 4, of the second epitaxial layer 6, of the regions 7, of the region 5 and of the regions 9, the combination of which allows the formation of the transistor Th, a formation of P-type regions 20 in the epitaxial layer portion comprised between the regions 9 occurs. In each region 20 couples of N-type regions 21 are formed and a formation of a gate structure 22 by means of an oxide layer 23 and a overlying polysilicon layer 24 occurs on the top surface of the chip, over the portion of epitaxial layer 6 which is comprised between the region 20.

The gate structure 22 represents the gate of the transistor Me in Figure 5 while the regions 20 represent the body region of the transistor Me and the regions 21 and 5 represent respectively the source and drain regions of the MOS transistor Me. The gate and source terminals Ge and Se are formed by means of a deposition of a metal layer 16 on bores formed by attacking the oxide layer 12 placed on the top surface of the chip.

Two polysilicon Zener diodes in back to back connection are formed over the top surface 400 of the chip after a deposition of a polysilicon layer 14 over a silicon oxide region 13 placed over a region 9 and an adjacent portion of the layer 6 which is allocated between said region 9 and a region 7 on the left part of the chip as showing the Figure 4. Such Zener diodes act as a quenching element B of the transistor Th.

Alternatively, instead of the two Zener diodes in back to back configuration, configurations comprising a single Zener diode or more than two Zener diodes as shown in Figures 6a-6d can be utilized for the integrated device in Figure 4.

In Figure 12 the output features measured for an emitter switching device as in Figures 4, 5 by imposing a control voltage Vgs=10V are shown.

An emitter switching device formed in a semiconductor substrate 2 with high N-type dopant concentration according to a third embodiment of the invention is

shown in Figures 7, 8. The integrated device shown in Figures 7, 8 is similar to the device shown in Figures 2, 3 but it differs for the use of two polysilicon Zener diodes Dz1, Dz2 in back to back connection as a quenching element, to which a diode Dh, which can be integrated in the same device or placed outside the chip and which is connected between the terminals Ch (collector terminal of the transistor Th) and Ee (emitter terminal of the transistor Te), is added and for the addition of control circuits not shown in Figures. Such control circuits integrated in the same chip are normally formed inside a P-type region 40 aligned to the region 4. The formation of such control circuits is accompanied by the presence of parasitic transistors formed, as showing Figure 8, for example, by a pnp transistor Qpar1 having the emitter terminal connected with the terminal Bh and the collector terminal connected with the P-type region 40 wherein are formed the control circuits, and which is connected with the base terminals of a series of bipolar transistors Qpar2a...Qpar2n the emitter terminals of which are connected with different supply voltages or coincide with the collector terminals of the npn transistors of the control circuits.

The integrated device in Figure 7 presents with respect to the device in Figure 2 other regions 40, 50, 70 which are similar to the region 4, 5, 7 and which are aligned to them and are formed in the right part of the chip as showing Figure 8. In such way the emitter and collector regions of the bipolar transistor Qpar1 are formed respectively by the regions 7 and 70 while the base region is formed by the portion of the layer 6 which is comprised between the layers 7 and 70. The emitter and base regions of the transistors Qpar2a...Qpar2n are given respectively by the layers 3 and the region 40 while the collector regions of the aforementioned transistors are given by different N-type regions similar to the region 50 (in Figure 7 only the transistor Qpar2a is shown).

The integrated device of Figures 7 and 8 is utilized above all in the case wherein the terminal Ch assumes negative voltage values. In this case the high voltage diode Dh goes in conduction when the voltage at the terminal Ch becomes negative with respect to the terminal Ee, put generally at ground. For a correct management of the control circuits the parasitic transistors Qpar2a...Qpar2n must never be turned on both in

direct conduction and in inverse conduction, that is with the substrate coinciding with the collector or with the emitter of the same parasitic transistor. The turning on of the transistors Qpar2a...Qpar2n occurs if the transistor Qpar1 goes in saturation region that is if the voltage value of the terminal Ch assumes a value equal to -[V1+V2+Vbe(Qpar1)] where V1 and V2 are the voltages at the terminals of the Zener diodes Dz1, Dz2 and Vbe(Qpar1) is the base-emitter voltage of the transistor Qpar1.

It is obvious that, in these bias conditions (with the terminal Ee positive with respect to the terminal Bh), the diode Dz1 is biased in the direct region of the diagram (V1=Vd1 0.6V), while the diode Dz2 is biased in the inverse region (V2=Vz2).

With respect to the electric configuration wherein the quenching element B is a simple Zener diode, as in the case of the previous indicated known art US 6127723, the above described configuration including the polysilicon diodes in back to back connection as a quenching elements, offers a notable advantage for the immunity against the turning on of the parasitic transistors Qpar2a...Qpar2n. In fact in the known art, the turning on of said parasitic transistors Qpar2a...Qpar2n would be obtained if the voltage of the terminal Ch assumes a value equal to -[Vd(B) + Vbe(Qpar1)], where Vd(B) is the direct bias voltage of the single Zener diode used as a quenching element.

An emitter switching device formed in a semiconductor substrate 2 with high N-type dopant concentration according to a fourth embodiment of the invention is shown in Figures 9, 10. The integrated device shown in Figures 9, 10 is similar to the device shown in Figures 7, 8 with only the difference of using the MOS transistor Me already shown in Figures 5, 6 and previous described as low voltage transistor. All the considerations made for the device according to the third embodiment of the invention are valid for the device shown in Figures 9 and 10.

A device in emitter-switching configuration according to a fifth embodiment of the invention is shown in Figures 11a and 11b. The integrated device shown in Figures 11a and 11b differs from the other embodiments for the presence of a power transistor in a Darlington configuration, that is it is formed by two high voltage bipolar transistors Th1 and Th2 which have the collector terminals in common and the emitter terminal of the

transistor Th1 connected with the base terminal of the transistor Th2. The latter can be connected with the anode of a diode D the cathode of which is connected with the base terminal Bh1 of the transistor Th1 as in Figure 11b or it can be connected with a quenching element B' connected with a not drivable terminal of the low voltage transistor (the bipolar transistor Te or the MOS transistor Me) indicated generally by the block 90, as in Figure 11a. All the considerations made for the devices according to the previous embodiments are valid for the device shown in Figures 11a and 11b.